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54 Video display apparatus.

57 A solid state light modulator apparatus is disclosed for displaying images represented by video signals. The system includes an array (11) of semiconductor devices having electrodes which extend over the tops of their respective devices. The devices are used, in conjunction with related circuitry, for applying sampled video signals to the electrodes. The resulting charge pattern deforms a conductive/reflective layer (14), and the deformations are converted to a viewable image by an optical system. In embodiments set forth, the electrodes are divided into separated fingers (300A, 300B) which decreases the effective grating line spacing of the light modulator and accordingly increases resolution. Also, in embodiments set forth, the electrodes are at two different levels, and the spurious light immunity of the light modulator is improved.

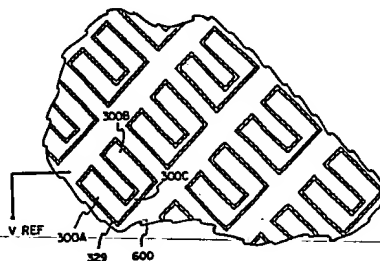


Fig. 6

Description

VIDEO DISPLAY APPARATUS

This invention relates to video display systems and, more particularly, to improvements in the type of video display which employs a deformable reflective surface having deformations that depend upon a stored charge pattern and an optical subsystem for converting the deformations into a viewable image.

There have been previously set forth techniques for displaying video information by storing a charge pattern representative of a video frame in a frame store and utilizing the charge pattern to modify a characteristic of a material. The modified characteristic of the material is then used to obtain a viewable image. For example, in U.S. Patent No. 3,882,271 there is disclosed a system called a solid state light modulator wherein a charge pattern on a special array of semiconductor devices is used to obtain deformations of a conductive reflective layer disposed over the array and spaced therefrom by an elastomer material such as silicone gel. An optical subsystem, such as a Schlieren optical system, can then be utilized to convert the pattern of deformations (or "ripples") in the reflective layer into a viewable image. The solid state light modulator is described further in U.S. Patent Nos. 4,529,620, 4,626,920, 4,639,788, and 4,641,193.

In U.S. Patent Nos. 4,639,788 and 4,641,193 there is disclosed a solid state light modulator which includes an array of columns and rows of devices in a semiconductor substrate. The devices comprise field-effect-transistors having spaced doped regions and a gate electrode disposed over an insulating layer that covers the area between the doped regions. A conductive so-called deflection electrode is coupled to one of the doped regions and has a top flat region which extends over its associated device and is spaced therefrom by an insulating material. The deflection electrodes are spaced from the conductive reflective layer by the elastomer, as mentioned above. The desired deformations of the conductive reflective layer are caused by the signals applied to the deflection electrodes. These signals are applied to the appropriate field effect devices, and the devices are switched on at the appropriate times by an addressing system.

In the described system, as set forth in the above referenced patents, the electrostatic force between each deflection electrode and the overlying portion of the conductive/reflective layer depends upon the voltage difference between the particular deflection electrode and the conductive/reflective layer. This force results in deformation of the conductive/reflective layer which, in turn, is ultimately converted by the optical system into an element of an image. Accordingly, it will be understood that the number of deflection electrodes in the array will determine the grating line spacing of the light modulator and, accordingly, the resolution capability of the system.

One method for increasing the number of deflection electrodes would be to increase the number of elements in the array, but it will be understood that

this would increase the cost and difficulty of fabrication. In addition to the obviously greater cost of providing more transistors and associated addressing circuitry, if the packing density of devices is increased, there will be a concomitant increase in the difficulty of designing and fabricating the array.

It is among the objects of the present invention to provide a device, of the general type described, which has improved resolution capability, but does not require a greatly increased number of switching devices in its array or unduly complicate the addressing system.

When making a solid state light modulator of the type described, one of the concerns is the intrusion of light from the imaging system onto the semiconductor devices of the array. The light to be reflected off the conductive/reflective layer of the solid state light modulator is very bright. The conductive/reflective layer cannot be too thick, since it must be deformable. Some of the intense light incident on the conductive/reflective layer is not reflected, and it passes through the conductive/reflective layer and the elastomer layer. Light that strikes certain regions of the semiconductor device can cause spurious switching and/or generation of signals that can degrade or ruin the image to be produced. In the above referenced U.S. Patent Nos. 4,639,788 and 4,641,193, the deflection electrodes substantially cover their respective semiconductor devices, and provide a degree of protection against the incursion of light. Also, a pattern of isolation electrodes are shown as being disposed between the deflection electrodes.

It is among the additional objects of the present invention to further improve the immunity of the solid state light modulator semiconductor devices against incursion of light from its optical system.

Four aspects of the invention are provided as defined by claims 1, 8, 14 and 19 respectively.

The present invention is directed to an improved video display apparatus for generating images represented by input video signals. The apparatus includes an array of semiconductor devices having respective electrodes to which charge is applied in accordance with the input video signals. A layer of deformable material is disposed over the electrodes, and a conductive/reflective (i.e., conductive and reflective) layer is disposed over the deformable layer. Optical means, such as a Schlieren optical system, are provided for converting deformations of the conductive/reflective layer into an image.

In accordance with an embodiment of the invention, each electrode of the array has a plurality of spaced conductive regions having respective surfaces of relatively large area in a common plane. The plurality of conductive regions of each electrode are electrically connected in common by at least one conductor having, at most, a relatively small area in said plane. Reference conductive regions have further surfaces in said plane, the further surfaces being between, and separated from, the surfaces of

the electrodes. At least some of the reference conductive regions are electrically coupled in common. Means are provided for applying input video signals to the electrodes of the array, and for applying at least one reference potential to the reference conductive regions.

As described further hereinbelow, in accordance with a feature of the invention as set forth, the improved electrode and reference conductor configuration results in a finer grating line spacing without increase of the number of devices in the array.

In accordance with a further embodiment of the invention, each conductive electrode has a first surface region at a first level above the semiconductor substrate and a plurality of further spaced apart surface regions at a second level above the first level. In this embodiment, reference conductive regions have surfaces at the second level which are disposed between the further surface regions of the electrodes and are separated therefrom. At least some of the reference conductors are connected in common. An additional advantage of this embodiment is the presence of conductors at two separated levels of the structure (the levels preferably being separated by insulating material such as silicon dioxide), which can serve to provide further protection against light from the optical system passing through the upper portions of the structure and striking the transistor devices.

In a still further embodiment of the invention, each electrode has a surface region at a first level above the semiconductor substrate. A plurality of reference conductive regions are located at a second level above said surface region of the electrode below, the levels again being separated by an insulating material. In this embodiment, however, the conductive regions at the second level are not coupled to the first level surface region of the electrode below. Rather, a reference potential is applied to the reference conductive regions. The reference conductive regions at the second level overlay only part of the electrode surface regions at the first level. As a result, each electrode is effectively divided into a plurality of portions which exert a force on the conductive/reflective layer (depending on the signal applied to the particular electrode) whereas, the reference conductive regions overlaying the regions between the stated portions exert a force on the conductive/reflective layer that depends on the reference potential applied to the reference conductive regions. This again results in an increase of the number of grating lines obtainable from an array of given number of electrodes. In a form of this embodiment, the conductive regions comprise a conductive layer at the second level, the conductive layer having a plurality of openings above each of the electrodes. The conductive layer can be divided into separate patterns above respective lines of the array, so that different reference potentials can be applied to different lines.

In still another embodiment of the invention, electrodes of the array have at least three electrically connected fingers such that at least one of the

fingers is interleaved with fingers of an electrode in a row above in said array and at least another of said fingers is interleaved with fingers of an electrode in a row below in said array. This electrode configuration permits application of input video signals and reference potential in a way which avoids a problem of undesired "memory" in the modulator structure (i.e. a persisting pattern in the conductive/reflective layer which can result in artifacts in the presented image) while maintaining the resolution of the displayed image.

Further features and advantages of the invention will become more readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Fig. 1 is a simplified diagram of a type of prior art apparatus for displaying images, in which the improvements of the invention can be made.

Fig. 2 is a block diagram, partially in schematic form, of a portion of a prior art apparatus.

Fig. 3 shows further detail of the semiconductor devices of the prior art apparatus.

Fig. 4 shows a cross sectional view of the prior art semiconductor devices of Fig. 3 as taken through the section defined by arrows 4-4 in Fig. 3.

Fig. 5 is a block diagram, partially in schematic form, of a portion of another prior art apparatus.

Fig. 6 shows a plan view of an electrode pattern and reference conductors in accordance with an embodiment of the invention.

Fig. 7 shows a variation of the Fig. 6 embodiment, with a different arrangement of reference conductors.

Fig. 8 shows a cross-sectional view of the devices of an array in accordance with a further embodiment of the invention.

Figs 9 and 10 show plan views of two arrangements of electrodes and reference conductive regions of the Fig. 8 embodiment.

Fig. 11 shows a cross-sectional view of the devices of an array in accordance with a still further embodiment of the invention.

Figs 12 and 13 show plan views of two arrangements of the reference conductive regions of the Fig. 11 embodiment.

Figs 14, 14A, 15 and 16 show electrode configurations in accordance with further embodiments of the present invention.

Referring to Fig. 1, there is shown a simplified schematic diagram of the type of apparatus 10 in which the improvements of the invention are made. A semiconductor substrate 11 has an array of devices formed in a surface 12 thereof, these devices serving as semiconductor controlled storage units. A layer of deformable material 13 (which may be, for example, an elastomer such as silicone gel) covers the surface 12, and a reflective layer 14 of conductive material is disposed over the deformable layer 13. The semiconductor device array, and associated circuitry 80, to be described further hereinbelow, receives and samples a video signal, the samples ultimately being stored as a charge pattern on the surface 12 of semiconductor 11. The electric field associated with the charge pattern results in a force with respect to the layer 14 which

deforms the deformable material 13 and layer 14 so that information is contained in the reflective layer 14 in the form of depressions or ripples which are similar to a phase diffraction grating. This information is then displayed on a screen 15, such as by using a Schlieren type of optical system.

The optical system depicted in Fig. 1 can be generally of the type disclosed in U.S. Patent No.s 3,084,590, 3,882,271, and 4,641,193. In this system arc electrodes 20 generate an intense light source that is directed by a curved mirror 21 over a masking system which includes a plurality of reflecting bars 23 separated by transparent areas or slits 24. The masking system 22 is positioned so that the light reflected from the bars 23 is transmitted toward a lens 25 where it is focused into parallel rays. These rays are incident on the deformed reflective surface 14 and are reflected back through the lens 25 toward the masking system. If, at a given instant, there were no depressions on the surface 14 to divert the light rays, the rays effectively emanating from each bar 23 would be focused by lens 25 on a bar and no light would be incident on the screen 15. However, if there are depressions in the surface 14 they will act as diffraction gratings and some light will be diffracted and ultimately pass through the slits 24. The portion of a light rays transmitted through a particular slit depends on the amplitude of the infinitesimal diffraction grating from which the ray was diffracted. Thus, an appropriate pattern of diffraction gratings, resulting from a selected charge pattern, will yield a desired image on the screen 15. The charge pattern is stored by the array of semiconductor devices, to be described, in the semiconductor substrate 11. In embodiments hereof, the array of semiconductor devices is arranged in a diagonal pattern, and the Schlieren bars are also oriented diagonally, as shown in Fig. 1.

Reference to prior art light modulator systems can be made to the abovereferenced U.S. Patent No. 3,882,271, and also to the U.S. Patent No. 4,441,791, which is of a different type in that it discloses a deformable mirror mounted on a grid over an array of semiconductor devices to form air-gap capacitors. Deformations of the mirror surface can be converted into an image by an optical system.

Referring to Fig. 2, there is shown an array of devices in semiconductor substrate 11. In the diagram of Fig. 2, each device or element 100 is illustrated by its deflection region 300, which is shown as being a square in the prior system, the squares being oriented and arranged in a diagonal pattern; i.e., with the deflection electrodes of each row of the array being offset horizontally with respect to its adjacent rows.

In the Fig. 2 system, the lines of elements 100 are numbered at the right of the Figure as line 1, line 2, etc., and illustrative elements from a central exemplary portion of the array are shown in Fig. 3 which shows a small portion of four consecutive lines designated using the generalized terminology of line j, line j+1, line j+2, and line j+3. In Fig. 2, the columns of the array are numbered as column 1, column 2, column 3, etc., and in Fig. 3 the columns

from a central exemplary portion of the array, are designated as column k, column k+1, column k+2, and column k+3. Each element of a column of the array is coupled in common, in a manner to be described, to a common column conductor 150 for that line, as seen in Figs 2 and 3. As seen in Fig. 2, the respective column conductors are coupled to respective sides of capacitors Co, the other sides of which are coupled to ground reference potential. [These and other groups of capacitors can be considered as storage registers, and it is noted that suitable analog registers (or digital registers in conjunction with conversion circuitry), such as charge coupled device registers, could alternatively be employed.] The column conductors and respective capacitors Co are also coupled, via respective switches 160, to respective sides of capacitors C1, the other sides of which are also coupled to ground reference potential. [Again, these capacitors can be considered as a storage register.] The switches 160 are simultaneously enabled by a signal derived from the horizontal sync signal, H. The capacitors C1 are also each coupled, via respective switches 165, to the output of another switch 170. The switches 165 are respectively enabled by signals on the output lines of respective stages of a shift register 180. The register 180 is loaded at one end (the right end in Fig. 2) with a logical "1" (high) level which is clocked through the register at a basic system element rate, from a clock, not shown. In the referenced U.S. patents, switch 170 is operative, under control of the output of flip flop 185, and the clock signal, to couple either the video input signal or ground reference potential to the inputs of switches 165. The vertical synchronizing signal, V, is utilized to set a different initial state of the flip flop 185 for the beginning of each scanline of a given field. In this manner, the switch 170 is used to load a scanline of information into capacitors C1 (via switches 165), under control of register 180, with successive samples of input video information alternating with ground reference potential.

The row conductors 330 are coupled to respective outputs of shift register 220, the outputs of register 220 being used to selectively enable the row conductors in sequence. The register 220 is clocked by the horizontal synchronizing signal, and is synchronized by the vertical synchronizing signal, V. At the beginning of each field, a signal derived from V is used to load the first stage of the shift register 220 with a logical "1" (high) level. At each horizontal scanline of the field, the logical "1" level is shifted to the next position in the register so that the row conductors are sequentially enabled, one line at a time.

In operation of the system of Figs 2 and 3, and as described in the referenced patents, a scanline of sampled video information is read sequentially into the capacitors C1 in alternation with ground reference potential. At the end of the scanline, a signal derived from the horizontal sync signal H is used to enable switches 160, so that the sampled video information (and gnd, as the case may be) in the capacitors C1 is coupled to respective capacitors Co and the respective column conductors 150. This

substantially stores the sampled elemental signals in capacitors Co where they are applied, during the next scanline (and while the next line of video information is being read into the respective capacitors C1), to the respective column conductors. The signal derived from H is also operative, at this time, to shift the register 220 so as to enable the next row conductor for the duration of the next line. The capacitors C1 and Co are charged (or discharged, as the case may be) through low impedances, so they can be charged in the relatively short durations during which their respective switches are enabled.

Each elemental signal can now be transferred into the respective deflection electrodes 300, of the two successive lines whose common row conductor has been enabled by the output of the register 220. Every other signal level entered in capacitors Co was at ground reference potential. Therefore, the video signal samples for the given scanline will be transferred into the respective deflection electrodes of one of the lines associated with the enabled row conductor, and ground reference potential will be transferred into each of the deflection electrodes of the other line which shares the energized row conductor.

During the transfer from the input capacitors Co to the respective deflection electrodes of the lines associated with the enabled row conductor, which occurs during approximately one scanline period, the next scanline of video information is being read into the capacitors C1 (again, in alternation with ground reference potential). In this manner, substantially a full scanline duration is available for transfer of the signal from the capacitors Co into the capacitance associated with the respective deflection electrodes. In particular, this capacitance comprises the capacitor formed by each deflection electrode 300 and the common electrode 14 (e.g. Fig.s 1 and 3) disposed above the deformable material (which is shown at ground reference potential in this example, but which can be operated at a negative bias voltage, as described in the referenced patents), and stray capacitance. In copending U.S. Patent Application Serial No. 053,572, assigned to the same assignee as the present application, there is disclosed a technique wherein the impedance in each column conductor between the input capacitor and its associated deflection electrodes is caused to vary in accordance with the change in video signal level from frame to frame, so as to achieve video noise reduction.

Fig.s 3 and 4 illustrate the configuration, as set forth in the referenced patents, of the devices 100 formed in the semiconductor substrate. The substrate is n-type silicon, and the regions 310 and 320 are spaced p-type diffusions, for example boron diffusions. The regions 310 are coupled to associated column conductors 150. The regions 320 are coupled to the respective deflection electrodes 300. An insulating region 325, typically a silicon dioxide layer, covers the semiconductor region between diffusions 310 and 320. The respective row conductors 330 are disposed above oxide layers 325, of the devices of their associated rows and serve as gates which, when energized or enabled, cause p-channel

conduction between the regions 310 and 320 so that the signals on the column conductor lines are effectively coupled to the deflection electrodes 300 of the devices on the enabled rows. The deflection electrodes 300 have top flat regions which extend over their associated devices and are spaced therefrom by insulating material such as silicon dioxide 329. The row switching, at the line rate of operation, permits use of polysilicon, while the faster column switching employs metal conductors in the present embodiments.

In the system of Fig.s 2-4, as set forth in the referenced patents, the system clock rate used to clock the sampled video signal into the storage capacitors (and ultimately into the array) is twice the rate at which video information is being entered, since half the time is being used to clock ground reference potential into every other horizontal element of a line. As described in the referenced patents, by using the system illustrated in Fig. 5, a clock rate can be used which is the same as the rate at which information is entered into the array. The device display electrodes of Fig. 5 are shown as being in the same general configuration as in Fig. 2. The row conductors 530 are coupled to the outputs of a shift register 520, and operate like their counterparts in Fig. 2 to sequentially enable row pairs of devices. The column conductors 551 of the odd columns are coupled to circuitry similar to that of Fig. 2; namely, to respective capacitors C2a, respective switches 560 that are again enabled by a signal derived from the horizontal sync signal H, respective capacitors C2b, and respective switches 565 which are enabled by respective outputs of shift register 580, which is clocked at the basic system clock rate and operates to successively enable the switches 565. The input to switches 565 is the output of a switch 585 which passes the input video signal during odd video fields and passes ground reference potential during even video fields.

The even column conductors 552 are coupled to similar circuitry which includes respective capacitors C3a, respective switches 570 that are enabled by a signal derived from the horizontal sync signal H, respective capacitors C3b, and respective switches 575 which, again, are sequentially enabled by respective output stages of a shift register (590) which is clocked at the basic system clock rate and operates to successively enable the switches 575. The input to switches 575 is the output of a switch 595 that is operative to pass the input video signal during even video fields and ground reference potential during odd video fields of a video frame. In the system of Fig. 5, the clock rate used can be half of that which was employed in the Fig. 2 embodiment, since the odd and even subsystems are utilized simultaneously to read in and transfer sampled input video signals and ground reference potential (as the case may be) into respective odd and even rows of the array devices.

In operation of the system of Fig. 5, during an odd video field the switch 585 is operative to pass the input video signal so that, for example, during the first video scanline the input video signal is sampled, under control of shift register 580, and stored in

capacitors C2a. Simultaneously, switch 595 is passing ground reference potential, which is being read into capacitors C3a under control of shift register 590. At the end of the first scanline, the switches 560 and 570 are momentarily enabled to transfer the signals from capacitors C2a into respective capacitors C2b, and to transfer the signals from capacitors C3a into capacitors C3b. The first row conductor 530, which is coupled to the devices of lines 1 and 2 of the array (as in the previous embodiment) is also enabled (and remains enabled during the next scanline, during which the sampled video signals (or ground reference potential, as the case may be) in capacitors C2b and C3b are transferred into the respective display electrodes of lines 1 and 2 of the array. During the next video field, the odd and even line conductors (and their associated circuits) reverse roles (by virtue of switching the status of switches 585 and 595) and ground reference potential is transferred into line 1 while the sampled video signal is transferred into line 2. It is noted in the referenced patents that a separate switching arrangement, such as for directly switching ground reference potential to the appropriate activated row, could be used.

Embodiments of the invention will now be described. In the embodiment of Fig. 6, each of the electrodes 300 (e.g. are coupled to diffusion region 320 in Fig. 4) comprises a pair of relatively large area conductive regions 300A and 300B, which are connected by narrow conductive region 300C. The regions 300A and 300B can be envisioned as a pair of electrode "fingers", which are at the same potential. In the Fig. 6 embodiment, most of the remaining surface around the electrodes is occupied by reference conductors which are represented by the common metalization 600 that can be coupled to a suitable referenced potential, V_{ref} . The reference conductors are separated from the electrodes, the silicon dioxide 329 below (see also Fig. 4) being visible between the separations in Fig. 6.

In operation, the signal on each electrode (as compared to the reference potential on the common metalization 600) will cause forces on the conductive/reflective layer 14 (e.g. Fig. 4), and will result in image formation with twice as many grating lines for the same number of electrodes, due to the presence of the spaced electrode fingers. It will be understood that in the addressing of the individual electrodes, since a reference potential (V_{ref} in Fig. 6) is applied to the reference conductors, it is not necessary to insert ground reference potential into every other line, and each row of electrodes will be individually addressed.

In the embodiment of Fig. 6, if the signals applied to the reference conductors are the same and the signals applied to the electrodes are of the same polarity over a period of time, the light modulator can suffer from a permanent "memory"; that is, a permanent or semi-permanent pattern of protrusions and/or depressions in the conductive/reflective layer (and the elastomer layer below) which result from deflection of particular regions of the conductive/reflective layer 14 always being in the same direction. This can result in artifacts in the

ultimately presented image.

One way of alleviating the "memory" problem is to vary the polarity of the signals applied to the electrodes of the array. For example, in the embodiment of Fig. 6, during one frame the input video signal can be applied with a black-to-white polarity in one direction (for example, with 0 volts as black and 20 volts as white), and during the next video frame, the input video signal can be applied with black-to-white polarity in the opposite direction (for example, with black at 0 volts and white at -20 volts).

The application of a different polarity of input signals to the electrodes during successive frames is useful in alleviating the problem of undesired "memory" of the modulator structure. However, the need to have voltage variations over a wider range (as in the example above) may be problematic.

Fig. 7 illustrates another embodiment of the invention which provides a solution to the stated problem. In this embodiment, the electrodes 300 are of the same configuration as in the Fig. 6 embodiment. However, in this case, the common metalization which comprises the reference conductors is divided so that individual scanlines of elements can have reference conductors at different reference potentials, for example V_1 for one line and V_2 for the next line, as shown in Fig. 7. [Three separated reference conductors 601, 602 and 603 are shown in Fig. 7, with 602 being shaded for clarity of illustration.] Another way of applying the input video signal would utilize the same range of voltages during successive frames, but would alter the reference potential applied to the reference conductors during successive frames, and would also reverse the polarity of the video signal applied to the electrodes during successive frames (or other desired periods). For example, if the voltage on the conductive/reflective layer 14 is a negative bias potential $-V_b$ (see, for example, U.S. Patent No. 4,639,788), during one frame the reference potential applied to the reference conductors could be 0 volts, with the applied video signal varying between 0 volts (for black) and 20 volts (for white); whereas, during the next frame the reference potential could be 20 volts, with the applied video signal varying between 20 volts (for black) and 0 volts (for white). In this arrangement, since the picture information for each line is retained for a full field, the reference potentials should be switched, a line at a time, as each new line of video information is read into the array. This is achieved in the embodiments of Figs. 7, 10 and 13 hereof by separately connecting the reference conductors associated with each line of the array. A suitable flip-flop and switch (as first illustrated above) can be used to select the reference potentials, which can then be read in, a line at a time in conjunction with the video, using a register, in the manner first shown hereinabove. The means for selection of desired black and white levels, and the polarity of the video signals, is well known in the art.

Referring to Fig. 8, there is shown a further embodiment of the invention, wherein each of the electrodes 300 has conductive regions at two different levels. The elements in Fig. 8 which are of like reference numerals to elements of Fig. 4 serve

the same or similar function. In Fig. 8, however, each of the electrodes 300 has a surface region 300G at a first level above the semiconductor substrate (and above its respective semiconductor device, in the illustrated configuration), and a pair of further spaced apart surface regions 300H and 300J at a second level above the first level, and connected thereto by vertical extensions 300M and 300N. The two levels are separated by an insulating layer 829 of silicon dioxide. The conductive region 300G, at the first level, is preferably of substantial area, so as to help prevent spurious light from reaching the semiconductor surface. If desired, reference conductive regions can also be provided at the first level. Reference conductive regions 800 are provided at the second level. The pattern of electrodes and reference conductive regions can be as shown in Figs. 9 and 10; i.e., similar to Figs. 6 and 7, respectively, but with no need for connection between the electrode fingers at the second level (since they are connected from below).

Operation of the embodiments illustrated in Figs. 8-10 is similar to the operation described with reference to Figs. 6 and 7, except that the electrodes and reference conductive regions are at the second level. They exert their forces on the conductive/reflective layer 14, as previously described, by virtue of the signals applied thereto. Although a further level of metallization is needed (as compared to the embodiments of Figs. 6 and 7), there is improved light immunity, and the exposed connections between electrode fingers (e.g. 300C in Fig. 6 or 7) are eliminated.

In the embodiments of Figs. 11-13 the electrodes are at a first level and the second level contains only reference conductive regions. As shown in Fig. 11, for example, the electrodes 300 can be in a configuration similar to that illustrated in conjunction with Fig. 4. In this case, however, reference conductors 910 are seen to be provided at the second level, which is again separated from the first level by an insulating layer (929). The reference conductors 910 are seen to overlay only a portion of an electrode or electrodes 300. A reference potential (in Fig. 12, or reference potentials, in Fig. 13) are applied to the reference conductive regions. Due to the presence of the reference conductive regions, the plurality of portions of each electrode (there being division into two portions in this case, although division into more portions can be employed, if desired) results in the exposed portions of each electrode (i.e., those portions which are not covered by a reference conductive region) exerting a separate force with respect to the reflective/conductive layer 14. This results in a doubling (in this case) of the number of grating lines obtained from the array. In the embodiment of Fig. 12, the reference conductive electrodes are all coupled together in a common metallization, and a pair of spaced apertures, which are rectangular in this illustration, are positioned over two regions of each electrode. In Fig. 12, two of the apertures are also designated by reference numerals 901 and 902, and these are shown in the crosssection of Fig. 11. The dashed lines in Fig. 12 illustrate the electrode 300

below.

In the embodiment of Fig. 13, the reference conductive regions associated with each scan line are separate (as in the prior embodiments of Figs. 7 and 10), so that different reference potentials can be applied to different lines.

Figs. 14-16 illustrate electrode configurations in accordance with a further embodiment of the present invention. In the embodiment of Fig. 14, which is preferred for displaying diagonally sampled signals, each conductive electrode 1400 has a central vertical portion 1410, and three generally rectangular horizontal fingers 1411, 1412, and 1413. If an element 1400 is considered to be on line (or row) j , at which its central finger 1412 is located, then its uppermost finger 1411 is seen to be interleaved with the two lower fingers of the adjacent electrodes in the row above, i.e., row $j-1$. Also, its lowermost finger 1413 is interleaved with the two upper fingers of the adjacent electrodes in the row below. The electrodes of the array are spaced slightly apart, and the insulator below (e.g. silicon dioxide 329 of Fig. 4) is visible between the electrodes. In operation, and as disclosed in U.S. Patent No.s 4,639,788 and 4,641,193, a reference potential can be applied to, say, odd numbered lines and input video applied to even numbered lines during one field, and then during the next field a reference potential can be applied to even numbered lines and input video applied to odd numbered lines. This avoids undesired "memory" in the modulator structure, as previously discussed. However, with previous electrode configurations this resulted in halving the grating wave length per pixel. The disclosed configuration, wherein fingers of an active electrode extend into the regions of the lines above and below, provides substantial improvement in this regard. The number of fingers can be increased, if desired, and the shape of the configuration can be modified, e.g. to minimize the width of the central vertical portion, (which does not contribute to the grating), as shown, for example, in Fig. 14A wherein the illustrated electrode has five fingers, two of which will be interleaved with fingers of electrodes in the row above, and two of which will be interleaved with fingers of the row below.

Figs. 15 and 16 show examples of electrode configurations which can be utilized in conjunction with cardinal sampling systems, and which have the same type of advantage as that just described. In Fig. 15, an electrode 1500 has a middle finger 1512 on a row j with its uppermost finger 1511 interleaved with fingers of the electrode of the row above (row $j-1$) and its lowermost finger 1513 interleaved with fingers of the electrode of the row below (row $j+1$). The fingers of row j (and other rows of the same odd/even sense) extend to the right of a vertical portion 1510, whereas the fingers of rows of the opposite sense (e.g. $j-1$, $j+1$, etc.) extend to the left of their vertical portion. The embodiment shown in Fig. 16 is similar, but the fingers of electrode 1600 form an S-shaped configuration, with two vertical portions. The vertical portion 1610A connects the central finger 1612 with the uppermost finger 1611, and the vertical portion 1610B connects the central

finger 1612 with the lowermost finger 1613.

The arrays of semiconductor devices hereof can be fabricated, for example, utilizing known semiconductor lithographic processes. Appropriate masks for the patterns of diffusions, electrodes, contacts, polysilicon and conductive layers, etc., are designed and utilized in sequences of selective diffusions, layer deposition, selective etching, electrode deposition, etc. (in the requisite order, as known in the art). The deformable layer 13 and conductive and reflective layer or layers 14 can be applied using techniques set forth, for example, in U.S. Patent No.s. 4,529,620 and 4,626,920, assigned to the same assignee as the present application.

The invention has been described with reference to particular preferred embodiments, but variations in for example, the number, orientation, and shape of the electrode fingers are possible.

Claims

1. Video display apparatus for generating images represented by input video signals, said apparatus including: an array of semiconductor devices having respective electrodes to which charge is applied in accordance with the input video signals; a layer of deformable material disposed over said electrodes; a conductive/reflective layer disposed over said deformable layer; and optical means for converting deformations of the conductive/reflective layer into an image characterised by each electrode of said array having a plurality of spaced conductive regions having respective surfaces of relatively large area in a common plane, the plurality of conductive regions of each said electrode being electrically connected in common by at least one conductor having, at most, a relatively small area in said plane; reference conductive regions having surfaces in said plane between the surfaces of said electrodes and separated therefrom, at least some of said reference conductive regions being electrically connected in common; and means for applying said input video signals to said electrodes of said array, and for applying at least one reference potential to said reference conductive regions.
2. A display apparatus as defined by claim 1, wherein the reference conductive regions are all electrically connected in common.
3. The display apparatus as defined by claim 1, wherein the reference conductive regions associated with the electrodes of individual lines of the array are electrically connected in common.
4. The display apparatus as defined by claims 1, 2 or 3, wherein said plurality of spaced conductive regions of said electrodes comprise spaced rectangular fingers.
5. The display apparatus as defined by claims 1, 2 or 4, wherein said electrodes are diagonally oriented in said array.
6. The display apparatus as defined by any of

claims 1 to 5, wherein said optical means comprises a Schlieren optical system.

7. The display apparatus as defined by claim 1, 3, or 5, wherein a layer of insulating material is disposed between the surface of said semiconductor and said common plane.

8. Apparatus for receiving video signals and displaying images represented by said video signals, comprising

a semiconductor substrate having an array of columns and rows of devices formed on a surface thereof, said devices comprising: a transistor formed in said substrate; a conductive electrode coupled to said transistor, said electrode having a first surface region at a first level above said semiconductor substrate and a plurality of further spaced apart surface regions at a second level above said first level;

reference conductive regions having surfaces at said second level between the further surface regions of said electrodes and separated therefrom, at least some of said reference conductive regions being electrically connected in common;

means for selectively applying said video signals to said transistors of said array and for controlling said transistors so as to selectively couple said video signals to said electrodes;

means, for applying at least one reference potential to said reference conductive regions;

a conductive/reflective layer spaced from said second level;

a layer of deformable material between said second level and said conductive/reflective layer; and means for converting deformations of said conductive/reflective layer into an image.

9. Apparatus as defined by claim 8, wherein insulating material is disposed between the surface of said semiconductor substrate and said first level, and insulating material is also disposed between said first level and said second level.

10. Apparatus as defined by claims 8 or 9, wherein the reference conductive regions are all electrically connected in common.

11. Apparatus as defined by claims 8 or 9, wherein the reference conductive regions associated with the electrodes of individual lines of the array are electrically connected in common.

12. Apparatus as defined by claims 8 or 9, wherein said plurality of spaced conductive regions of said electrodes comprise spaced rectangular fingers.

13. Apparatus as defined by claims 8 or 9, wherein said electrodes are diagonally oriented in said array.

14. Apparatus for receiving video signals and displaying images represented by said video signals, comprising:

a semiconductor substrate having an array of columns and rows of devices formed on a surface thereof, said devices comprising: a transistor formed in said substrate; a conductive electrode coupled to said transistor and having a surface region at a first level above said semiconductor substrate; and a plurality of reference conductive regions at a second level above said surface region; means for selectively applying said video signals to said transistors of said array and for controlling said

transistors so as to selectively couple said video signals to said conductive electrodes;
 means for applying at least one reference potential to said reference conductive regions;
 a conductive/reflective layer spaced from said second level;
 a layer of deformable material between said second level and said conductive/reflective layer; and
 means for converting deformations of said conductive/reflective layer into an image.

15. Apparatus as defined by claim 14, wherein insulating material is disposed between the surface of said semiconductor substrate and said first level, and insulating material is also disposed between said first level and said second level.

16. Apparatus as defined by claims 14 or 15, wherein said reference conductive regions overlay portions of the electrodes below.

17. Apparatus as defined by claims 14 or 15, wherein said reference conductive regions comprise a conductive layer at said second level, said conductive layer having a plurality of openings above each of said electrodes.

18. Apparatus as defined by claim 17, wherein said conductive layer is divided into separate patterns above respective lines of said array.

19. Video display apparatus for generating images represented by input video signals, said apparatus including: an array of semiconductor devices arranged in a pattern of rows and columns and having respective electrodes to which charge can be applied in accordance with the input video signals; a layer of deformable material disposed over said electrodes; a conductive/reflective layer disposed over said deformable layer; and optical means for

converting deformations of the conductive/reflective layer into an image; characterised by the electrodes of said array having at least three electrically connected fingers such that at least one of said fingers is interleaved with fingers of an electrode in a row above in said array and at least another of said fingers is interleaved with fingers of an electrode of a row below in said array; and means for applying video signals to said devices.

20. Apparatus as defined by claim 19, wherein said means for applying video signals comprises means for applying, during one display field, input video signals to devices of odd rows and a reference potential to devices of even rows, and for applying, during the next display field, input video signals to devices of even rows and a reference potential to devices of odd rows.

21. Apparatus as defined by claims 19 or 20, wherein said fingers are of generally rectangular shape.

22. Apparatus as defined by claim 21, wherein said fingers have their lengthwise dimensions in a direction parallel to said rows.

23. Apparatus as defined by claims 19, 20 or 21, wherein said electrodes comprise at least one portion extending vertically in said array, with fingers extending horizontally from said at least one vertical portion.

24. Video display apparatus comprising a combination of two or more of apparatus according to any of claims 1 to 7, apparatus according to any of claims 8 to 13, apparatus according to any of claims 14 to 18, and apparatus according to any of claims 19 to 23.

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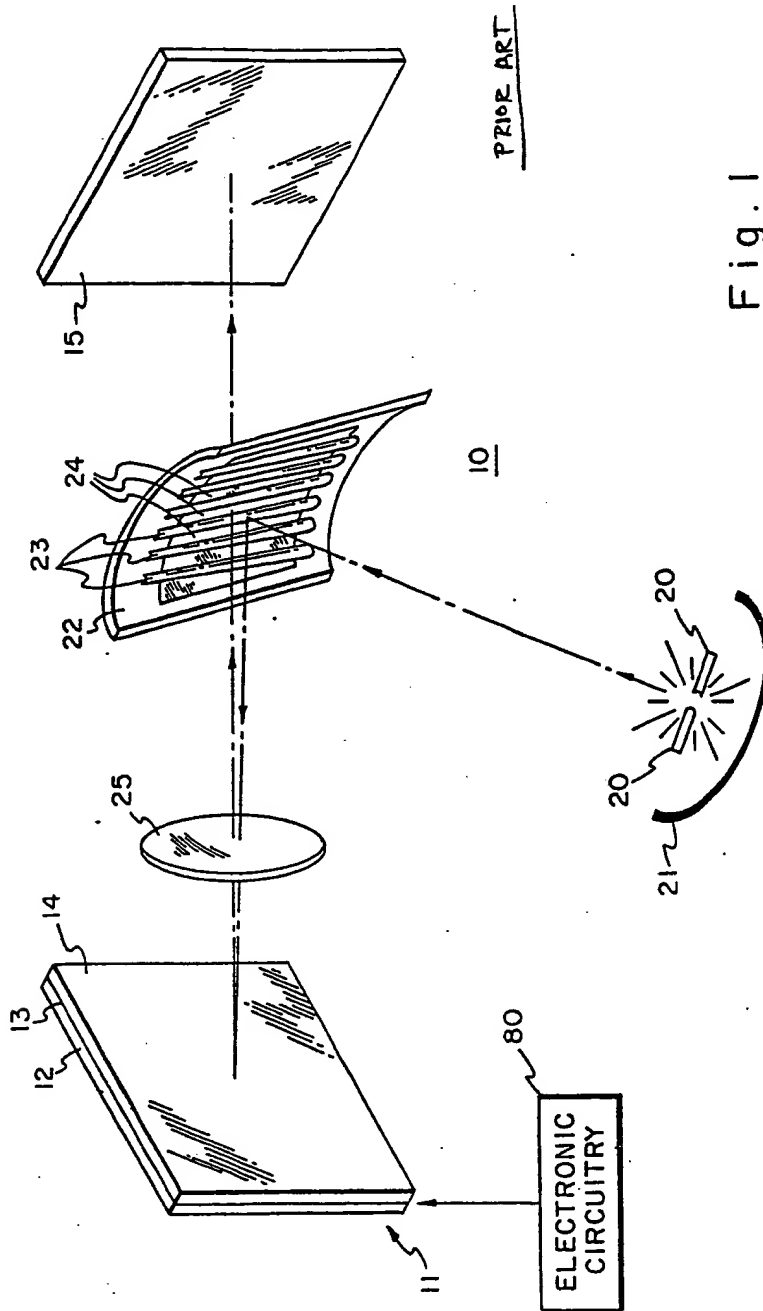
50

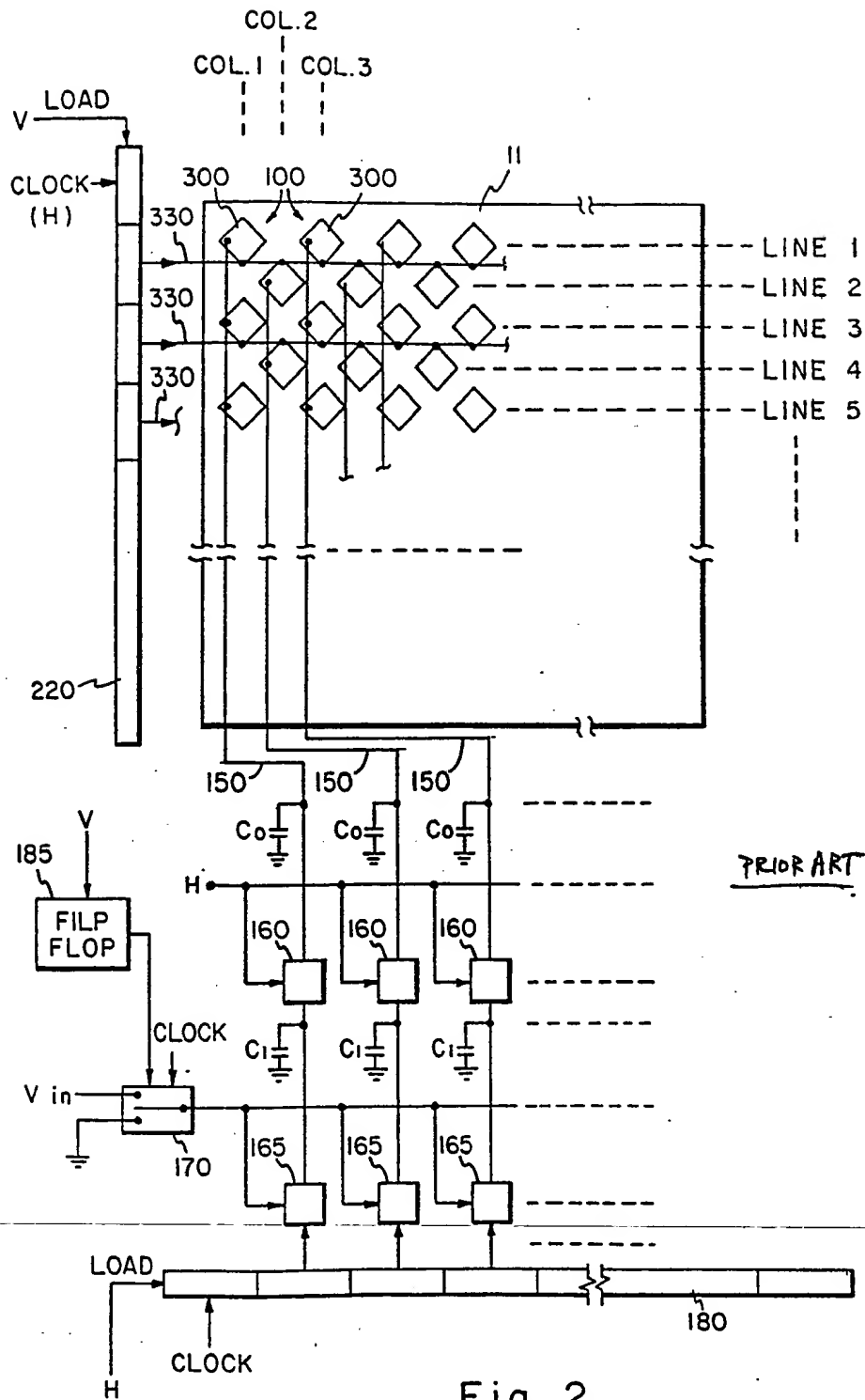
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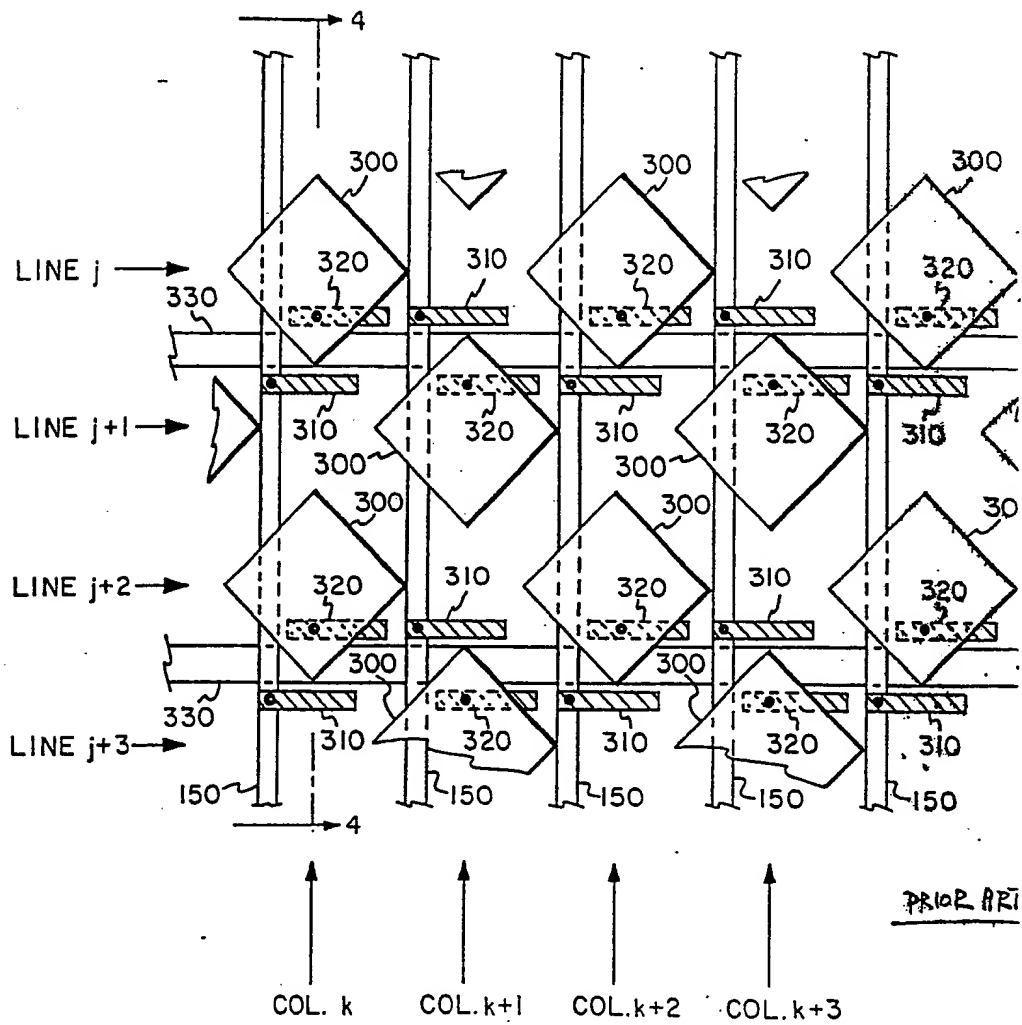


Fig. 3

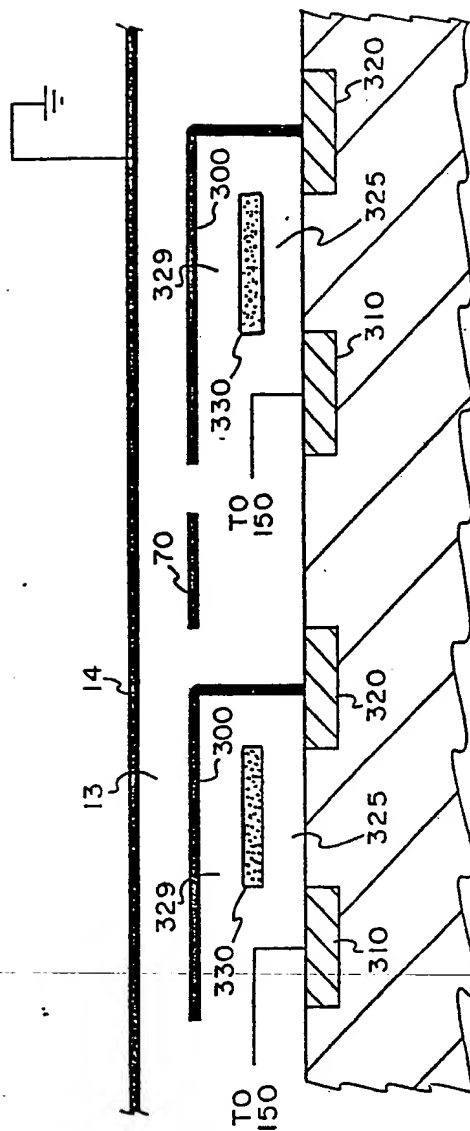
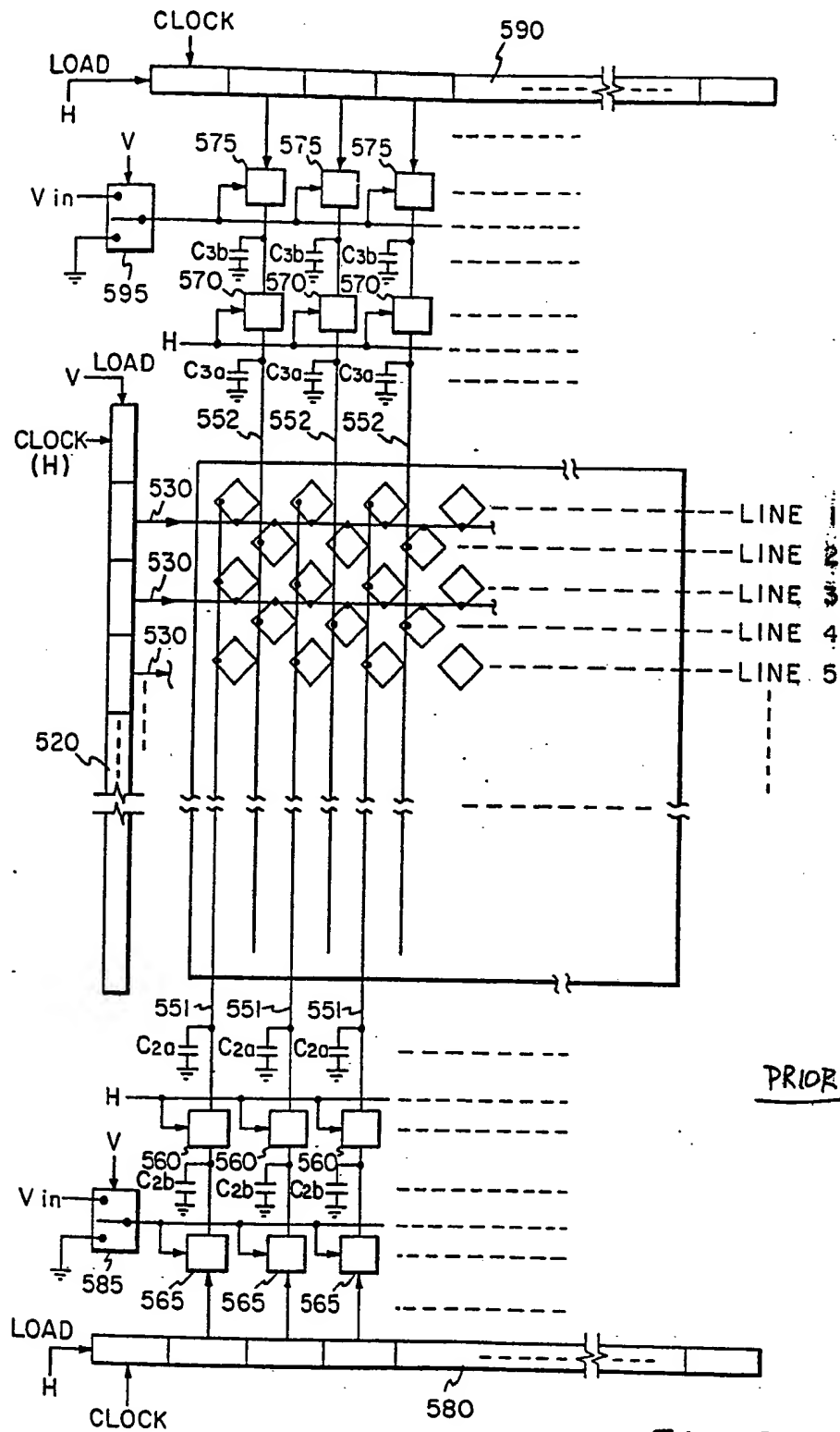


Fig. 4



PRIOR ART

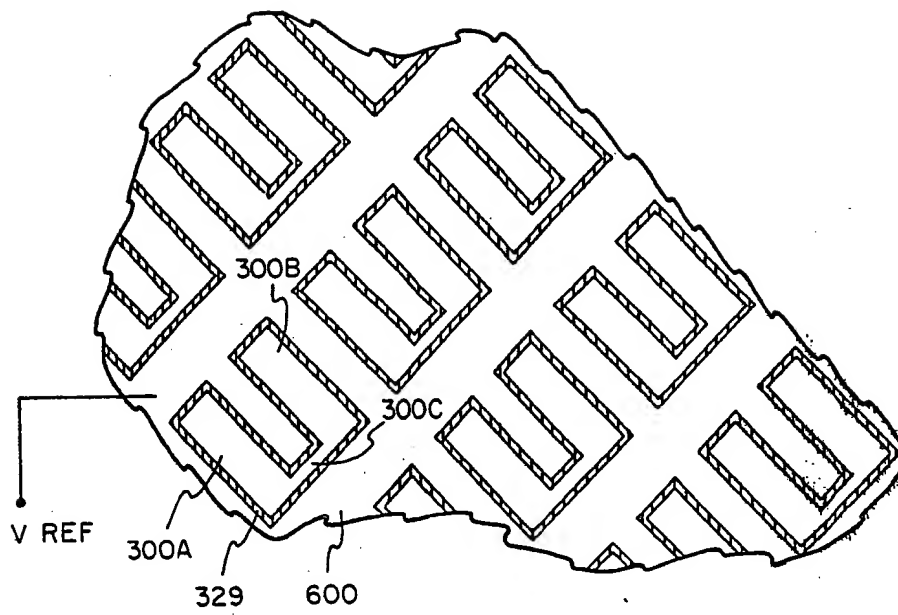


Fig. 6

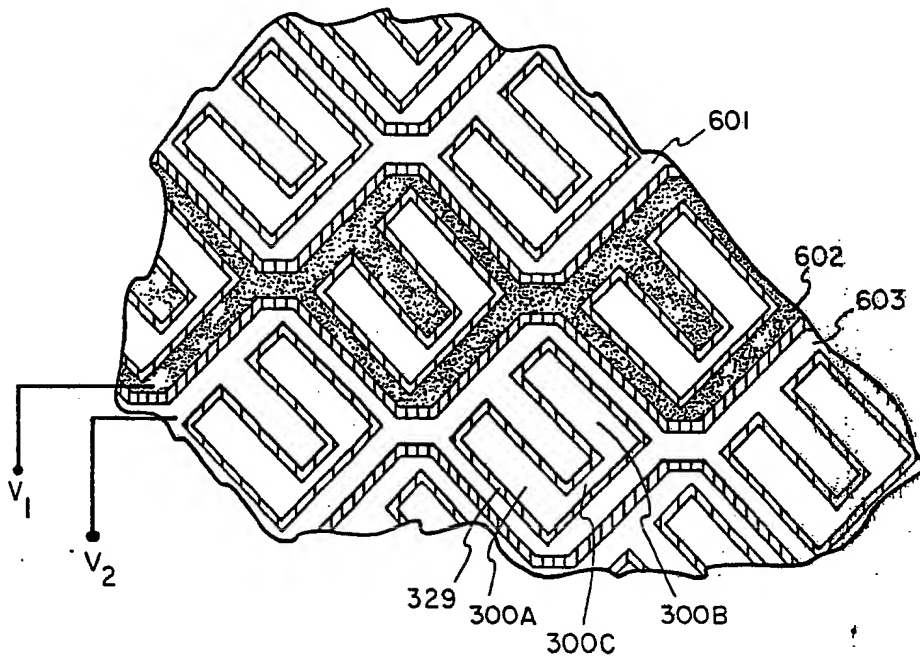


Fig. 7

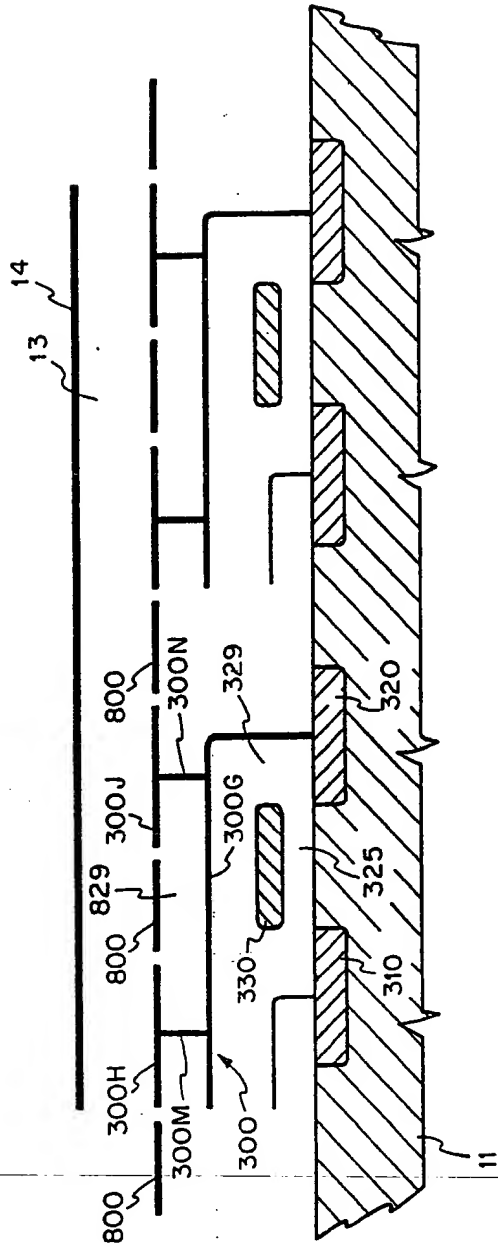


Fig. 8

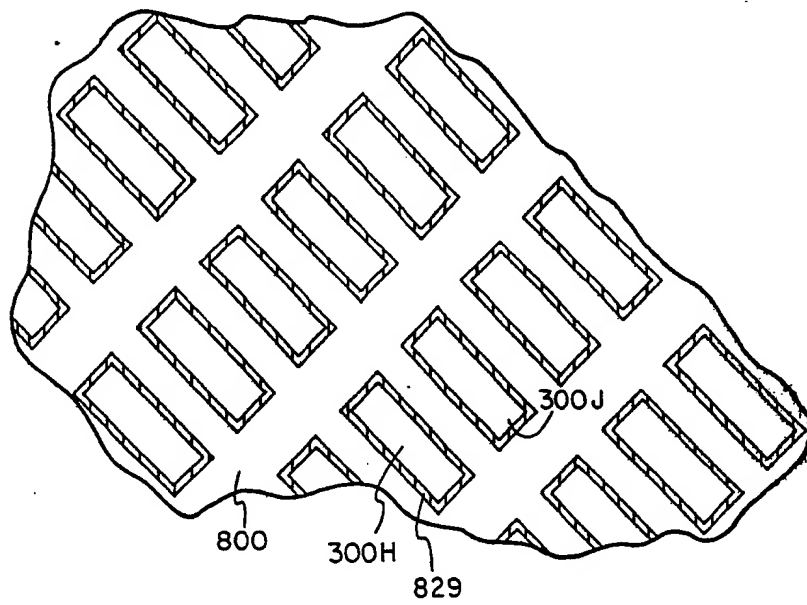


Fig. 9

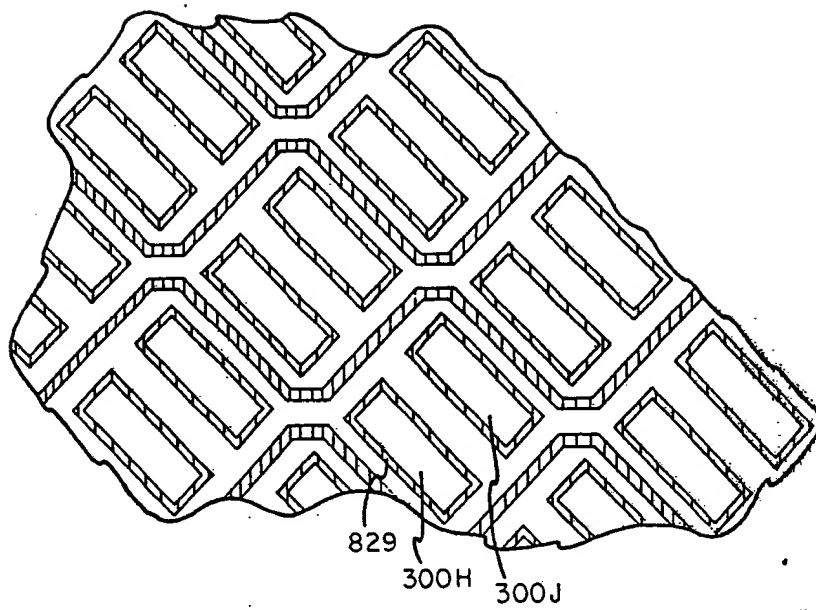


Fig. 10

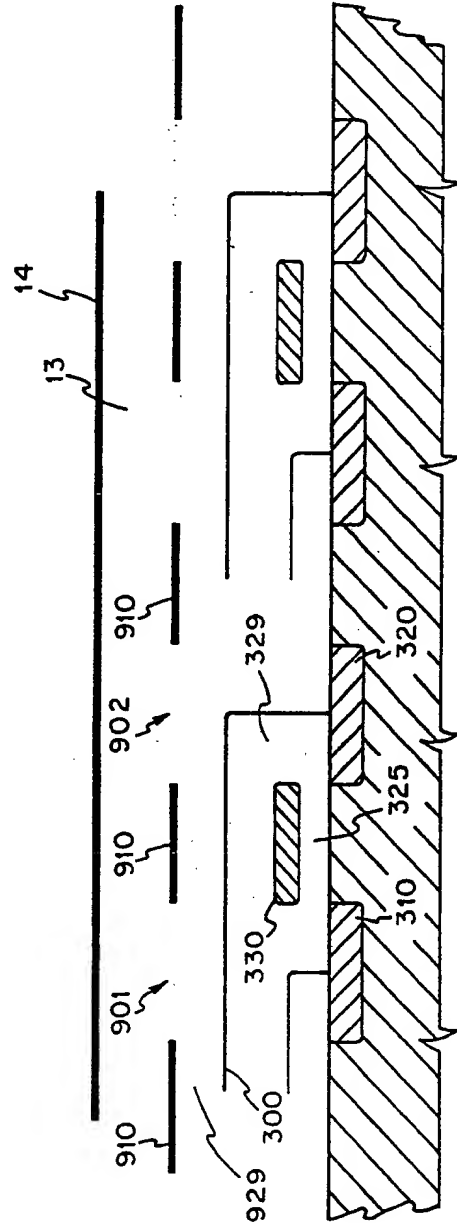


Fig. 11

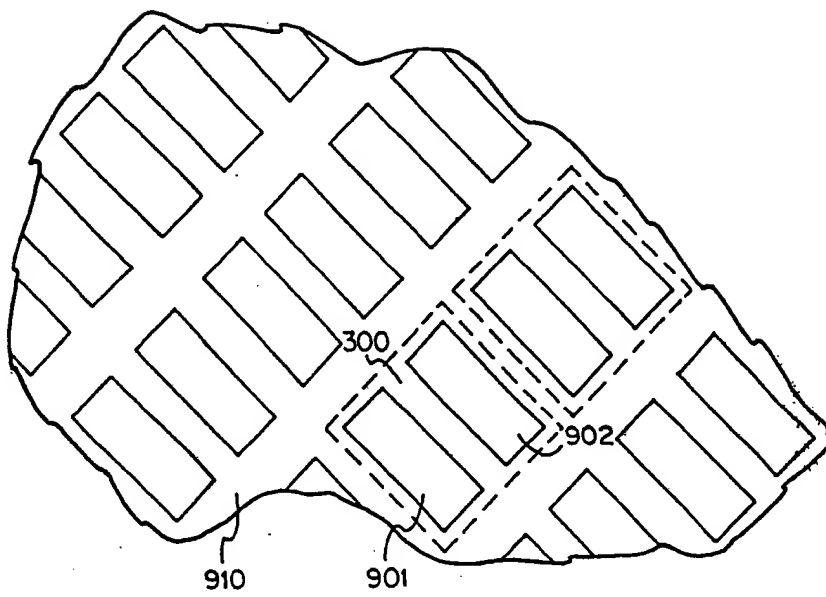


Fig. 12

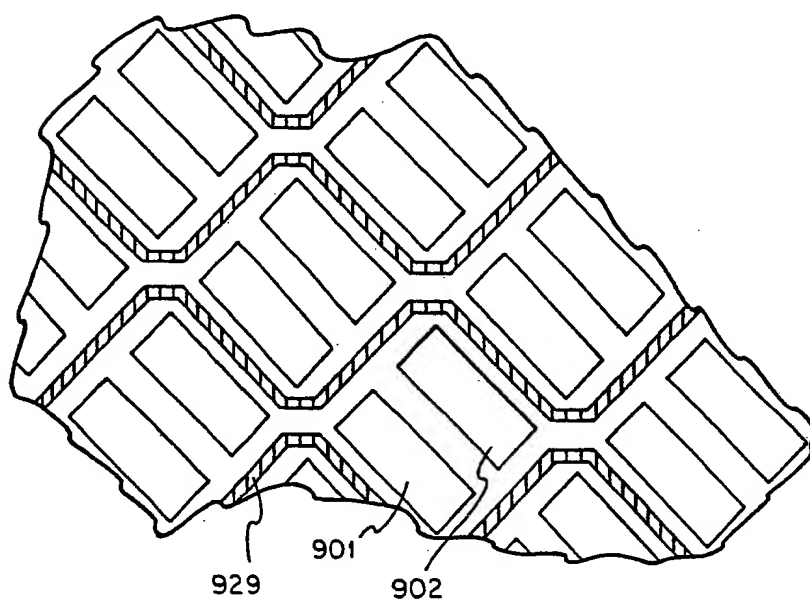


Fig. 13

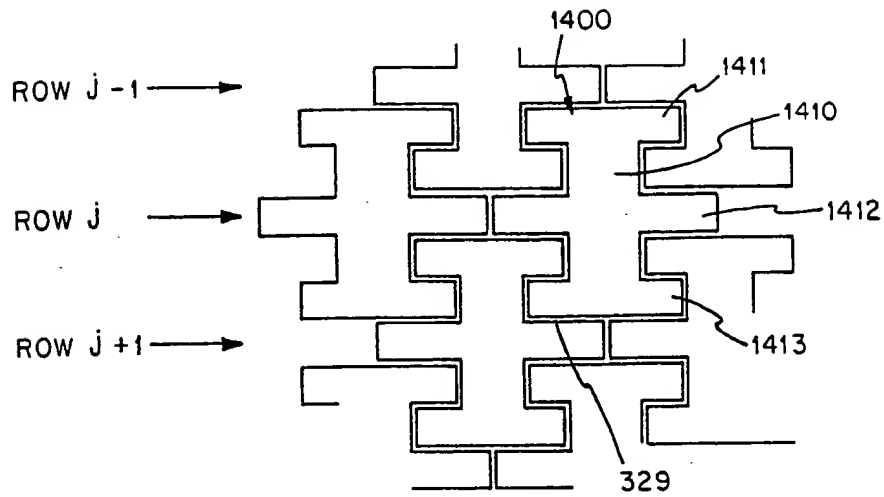


Fig. 14

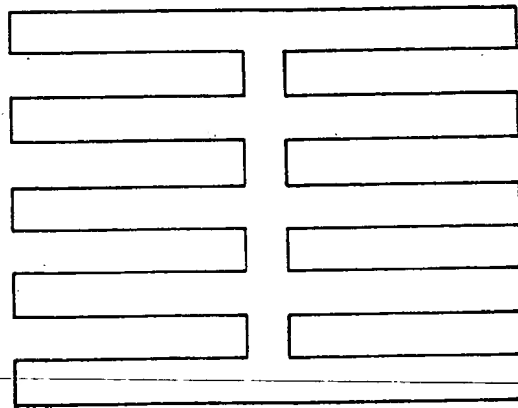


Fig. 14A

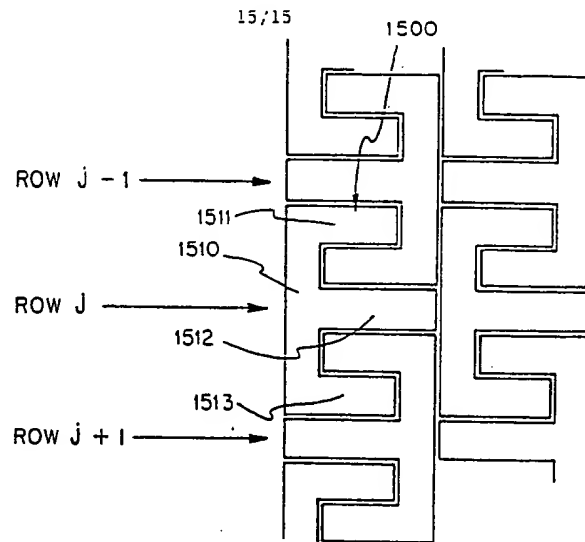


Fig. 15

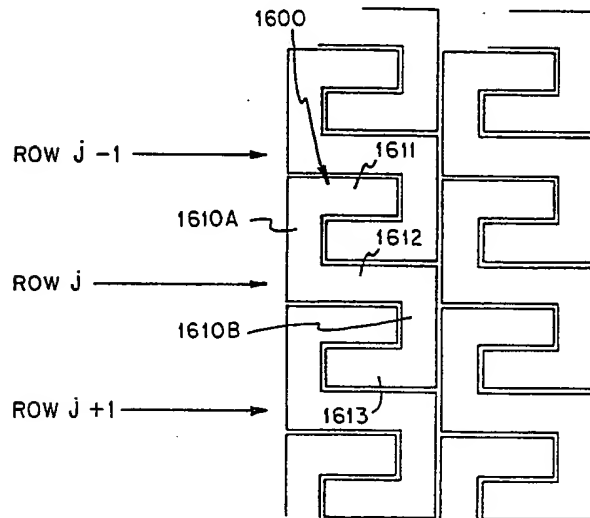


Fig. 16

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Video display apparatus.

A solid state light modulator apparatus is disclosed for displaying images represented by video signals. The system includes an array (11) of semiconductor devices having electrodes which extend over the tops of their respective devices. The devices are used, in conjunction with related circuitry, for applying sampled video signals to the electrodes. The resulting charge pattern deforms a conductive/reflective layer (14), and the deformations are converted to a viewable image by an optical system. In embodiments set forth, the electrodes are divided into separated fingers (300A, 300B) which decreases the effective grating line spacing of the light modulator and accordingly increases resolution. Also, in embodiments set forth, the electrodes are at two different levels, and the spurious light immunity of the light modulator is improved.

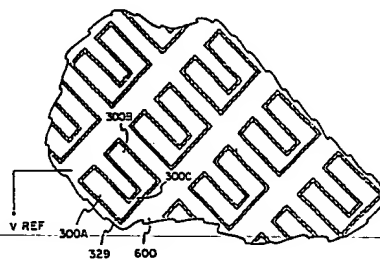


Fig. 6

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